



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Group Art Unit: 2818

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Examiner: A. Tran

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For: FLASH EEPROM SYSTEM

San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

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VOLUNTARY AMENDMENT

Sir:

Please add the following new claim:

--99. A non-volatile semiconductor memory system comprising:

a plurality of memory cells arranged into substantially a matrix pattern to construct a memory cell array, data being electrically erasable from and writable in each of said memory cells;

a plurality of bit lines each connected to said memory cells, each for transmitting a voltage corresponding to data to be written to one of said memory cells in which data are to be written in write mode and for receiving a voltage corresponding to data to be read from one of said memory cells from which data are to be read in read mode;

a plurality of data storing circuits each connected to each of said bit lines, for storing data to be written; in the write mode, the written data controlling voltage of said bit lines; and when data are read for write verify, levels of the data to be written and stored in said data storing circuits being determined, on the basis of the data read from said memory cells to which data have been